

IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the specification:

1-20 (Canceled).

21. (Previously Presented) A comparator cycling between an analog configuration and a digital configuration, said comparator comprising:

at least two transistors;

a plurality of transmission gates coupled to said transistors and adapted to select a reference signal and a comparator output signal for signal selection; and

a plurality of invertors coupled to said plurality of transmission gates, wherein said plurality of invertors are operable to buffer said comparator output signal, wherein the buffered output signal is returned as two signals to control said plurality of transmission gates,

wherein said comparator is set to have a first trip point associated with a rising edge of an input signal according to a value of a positive external voltage reference, and a second trip point associated with a falling edge of said input signal according to a width-to-length ratio of said transistors,

wherein only in said analog configuration one of said transistors is a tail current source transistor, whereby said input signal rises from ground toward a positive power supply voltage, and whereby the rise in said input signal switches said tail current source transistor off,

wherein one of said first or second trip point is set externally from said comparator, and

wherein a majority of a cycle time of said comparator is spent in said digital

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configuration.

22. (Previously Presented) The comparator of claim 21, wherein said rise in said input signal causes said comparator to appear as a differential pair in an open loop configuration.
23. (Previously Presented) The comparator of claim 21, wherein in said digital configuration, said input signal is at an input voltage level greater than a level of said positive external voltage reference.
24. (Previously Presented) The comparator of claim 23, wherein said input signal causes said comparator to have characteristics of an asymmetric inverting Schmitt trigger.
25. (Previously Presented) The comparator of claim 21, wherein said transistors comprise:
a first transistor of length (L_x) and a width of (W_x); and
a second transistor of length (L_y) and a width of (W_y),
wherein said width-to-length ratio equals $(W_x L_y)/(W_y L_x)$, and
wherein as said input signal decreases, a switching threshold becomes dependent on said width-to-length ratio.
26. (Previously Presented) The comparator of claim 21, wherein a level of said second trip point decreases by decreasing said width-to-length ratio.

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27. (Previously Presented) The comparator of claim 21, wherein a level of said second trip point increases by increasing said width-to-length ratio.
28. (Previously Presented) The comparator of claim 21, wherein said comparator spends approximately 80% of said cycle time in said digital configuration.
29. (Previously Presented) A comparator cycling between an analog configuration and a digital configuration, said comparator comprising:
- a plurality of transistors;
 - a plurality of transmission gates coupled to said transistors and adapted to select a reference signal and a comparator output signal for signal selection; and
 - a plurality of invertors coupled to said plurality of transmission gates, wherein said plurality of invertors are operable to buffer said comparator output signal, wherein the buffered output signal is returned as two signals to control said plurality of transmission gates,
- wherein said comparator is set to have a first trip point associated with a rising edge of an input signal according to a value of a positive external voltage reference, and a second trip point of a falling edge of the input signal according to a width-to-length ratio of said transistors,
- wherein a level of said second trip point is adjustable according to said width-to-length ratio,
- wherein only in said analog configuration, said device further comprises a tail current source transistor, whereby said input signal rises from ground toward a positive power supply voltage, and whereby said rise in said input signal switches said tail current source transistor off,

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wherein one of said first or second trip point is set externally from said comparator, and
wherein a majority of a cycle time of said comparator is spent in said digital
configuration.

30. (Previously Presented) The comparator in claim 29, wherein said transistors comprises:
a first transistor of length (L_x) and a width of (W_x); and
a second transistor of length (L_y) and a width of (W_y),
wherein said width-to-length ratio equals $(W_x L_y)/(W_y L_x)$, and
wherein as said input signal decreases, a switching threshold becomes dependent on said
width-to-length ratio.
31. (Previously Presented) The comparator of claim 29, wherein the rise in said input signal
causes said comparator to appear as a differential pair in an open loop configuration.
32. (Previously Presented) The comparator of claim 29, wherein in said digital configuration,
said input signal is at an input voltage level greater than a level of said positive external voltage
reference.
33. (Previously Presented) The comparator of claim 32, wherein said input signal causes said
comparator to have characteristics of an asymmetric inverting Schmitt trigger.
34. (Previously Presented) The comparator of claim 29, wherein said comparator spends

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approximately 80% of said cycle time in said digital configuration.

35. (Previously Presented) A comparator set to have a pair of trip points corresponding to a voltage value of a rising and falling edge of an input signal, wherein said comparator cycles between an analog configuration and a digital configuration by selective selection of said input signal through a plurality of transmission gates, wherein said comparator controls a delay between rising and falling edge transitions at an output signal of said comparator, wherein said comparator controls a pulse width at said output signal of said comparator, wherein one of said trip points is external to said comparator, and wherein a majority of a cycle time of said comparator is spent in said digital configuration.

36. (Currently Amended) ~~The comparator of claim 35,~~ A comparator set to have a pair of trip points corresponding to a voltage value of a rising and falling edge of an input signal, wherein said comparator cycles between an analog configuration and a digital configuration by selective selection of said input signal through a plurality of transmission gates, wherein said comparator controls a delay between rising and falling edge transitions at an output signal of said comparator, wherein said comparator controls a pulse width at said output signal of said comparator, wherein one of said trip points is external to said comparator, wherein a majority of a cycle time of said comparator is spent in said digital configuration, and wherein said analog configuration comprises:

an input signal terminal;

an output signal terminal;

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a positive power supply voltage terminal;

a positive external voltage reference terminal;

a tail current source transistor operatively connected to said positive power supply voltage terminal;

a first pair of transistors operatively connected to said tail current source transistor, said input signal terminal, and said positive external voltage reference terminal;

a second pair of transistors operatively connected to said first pair of transistors, wherein said second pair of transistors operate as current mirror load transistors; and

a plurality of invertors operatively connected to said output signal terminal, said first pair of transistors, and said second pair of transistors, wherein said plurality of invertors are operable to buffer said output signal, wherein the buffered output signal is returned as two signals to control said plurality of transmission gates.

37. (Currently Amended) ~~The comparator of claim 35,~~ A comparator set to have a pair of trip points corresponding to a voltage value of a rising and falling edge of an input signal, wherein said comparator cycles between an analog configuration and a digital configuration by selective selection of said input signal through a plurality of transmission gates, wherein said comparator controls a delay between rising and falling edge transitions at an output signal of said comparator, wherein said comparator controls a pulse width at said output signal of said comparator, wherein one of said trip points is external to said comparator, wherein a majority of a cycle time of said comparator is spent in said digital configuration, and wherein said digital configuration comprises:

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an input signal terminal;

an output signal terminal;

a positive power supply voltage terminal;

a tail current source transistor operatively connected to said positive power supply voltage terminal and said input signal terminal;

a first pair of transistors operatively connected to said tail current source transistor and said input signal terminal;

a current mirror load transistor operatively connected to said input signal source and said first pair of transistors; and

a plurality of invertors operatively connected to said output signal terminal, said first pair of transistors, and said current mirror load transistor, wherein said plurality of invertors are operable to buffer said output signal, wherein the buffered output signal is returned as two signals to control said plurality of transmission gates.

38. (Previously Presented) The comparator of claim 36, wherein in said analog configuration, said input signal rises from ground toward a positive power supply voltage, wherein said rise in said input signal switches said tail current source transistor off.

39. (Previously Presented) The comparator of claim 37, wherein in said digital configuration, said input signal is at an input voltage level greater than a level of said positive external voltage reference.

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40. (Previously Presented) The comparator of claim 35, wherein said comparator spends approximately 80% of said cycle time in said digital configuration.

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